

CLAIMS

What is Claimed is:

1. A semiconductor device having a surface, comprising:
a plurality of conductive sub-surface regions of a first conductivity each formed
5 beneath said surface, wherein said conductive sub-surface regions form a sub-surface
structure having a first RC property; and
a metal mesh structure formed above said surface, wherein said metal mesh
structure is coupled to said sub-surface structure via a plurality of spaced tap contacts,
and wherein said sub-surface structure and said metal mesh structure form a
10 combined structure having a second RC property that is lower than said first RC
property.
2. The semiconductor device as recited in Claim 1 wherein said sub-
surface structure is a diagonal sub-surface mesh structure.
- 15 3. The semiconductor device as recited in Claim 1 wherein said sub-
surface structure is an axial sub-surface mesh structure.
4. The semiconductor device as recited in Claim 1 wherein said sub-
20 surface structure is a diagonal sub-surface strip structure.
5. The semiconductor device as recited in Claim 1 wherein said sub-
surface structure is an axial sub-surface strip structure.

6. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has an N-type doping.

5 7. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a P-type doping.

8. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a strip shape.

10 9. The semiconductor device as recited in Claim 1 wherein said combined structure routes a single body-bias voltage.

10. The semiconductor device as recited in Claim 1 wherein said combined
15 structure routes a plurality of body-bias voltages.

11. A semiconductor device having a surface, comprising:
a plurality of conductive sub-surface regions of a first conductivity each formed
beneath said surface, wherein said conductive sub-surface regions form a sub-surface
20 structure having a first RC property; and

a metal ring structure formed above said surface, wherein said metal ring structure is coupled to said sub-surface structure via a plurality of spaced tap contacts,

and wherein said sub-surface structure and said metal ring structure form a combined structure having a second RC property that is lower than said first RC property.

12. The semiconductor device as recited in Claim 11 wherein said sub-
5 surface structure is a diagonal sub-surface mesh structure.

13. The semiconductor device as recited in Claim 11 wherein said sub-surface structure is an axial sub-surface mesh structure.

10 14. The semiconductor device as recited in Claim 11 wherein said sub-surface structure is a diagonal sub-surface strip structure.

15 15. The semiconductor device as recited in Claim 11 wherein said sub-surface structure is an axial sub-surface strip structure.

16. The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has an N-type doping.

17. The semiconductor device as recited in Claim 11 wherein each
20 conductive sub-surface region has a P-type doping.

18. The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has a strip shape.

19. The semiconductor device as recited in Claim 11 wherein said combined structure routes a single body-bias voltage.

5 20. The semiconductor device as recited in Claim 11 wherein said combined structure routes a plurality of body-bias voltages.

21. A semiconductor device having a surface, comprising:
a plurality of conductive sub-surface regions of a first conductivity each formed
10 beneath said surface, wherein said conductive sub-surface regions form a sub-surface structure having a first RC property; and
a metal branching tree structure formed above said surface, wherein said metal branching tree structure is coupled to said sub-surface structure via a plurality of spaced tap contacts, and wherein said sub-surface structure and said metal branching
15 tree structure form a combined structure having a second RC property that is lower than said first RC property.

22. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is a diagonal sub-surface mesh structure.

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23. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is an axial sub-surface mesh structure.

24. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is a diagonal sub-surface strip structure.

25. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is an axial sub-surface strip structure.

26. The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has an N-type doping.

27. The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has a P-type doping.

28. The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has a strip shape.

29. The semiconductor device as recited in Claim 21 wherein said combined structure routes a single body-bias voltage.

30. The semiconductor device as recited in Claim 21 wherein said combined structure routes a plurality of body-bias voltages.